

WHAT IS CLAIMED IS:

1. A clock control circuit carrying out control of a clock signal supplied to a central processing unit, the clock control circuit comprising:

a high-speed clock source whose oscillation operation is controlled by an operation control signal, and which generates a high-speed clock used in a usual operation mode;

a low-speed clock source always generating a low-speed clock whose frequency is lower than a frequency of the high-speed clock;

a selector selecting one of the high-speed clock and the low-speed clock in accordance with a selection signal, and outputting the selected one of the high-speed clock and the low-speed clock to the central processing unit;

a first control section which, when a standby mode is designated by a mode signal, outputs the operation control signal for stopping the high-speed clock source, and which, when an interrupt signal is supplied, outputs the operation control signal for operating the high-speed clock source; and

a second control section which, when the standby mode is designated by the mode signal, outputs the selection signal for causing the low-speed clock to be selected, and which, when the interrupt signal is supplied, starts counting of the low-speed clock, and when a count value reaches a value set in a register, the second control section outputs the selection signal for

causing the high-speed clock to be selected.

2. The clock control circuit of claim 1, further comprising an interrupt signal control section which selects an arbitrary one of or plurality of signals from a plurality of interrupt cause signals, and when a cause for interruption arises at any of the selected signals, the interrupt signal control section outputs the interrupt signal.

3. The clock control circuit of claim 1, wherein the first control section includes an OR gate to which a reset signal and the interrupt signal can be inputted, and a flip-flop which can be connected to an output side of the OR gate.

4. The clock control circuit of claim 1, wherein the second control section includes an OR gate to which a reset signal and the selection signal can be inputted, a flip-flop which can be connected to an output side of the OR gate, an AND gate which can be connected to an output side of the flip-flop, and a counter which can be connected to an output side of the AND gate, and the low-speed clock can be inputted from the low-speed clock source to the AND gate, and the counter carries out the counting of the low-speed clock.

5. The clock control circuit of claim 1, wherein, in order to switch

between clocks of two systems, the selector includes a two-input OR gate, a two-input AND gate, a flip-flop having a reset input, a low-through latch, and an inverter.

6. The clock control circuit of claim 1, wherein the high-speed clock source includes an oscillator, and a multiplier which multiplies by a predetermined number the high-speed clock outputted from the oscillator.

7. The clock control circuit of claim 1, wherein the high-speed clock source includes an oscillator, and a frequency divider which processes the high-speed clock outputted from the oscillator.

8. The clock control circuit of claim 1, wherein the selector is disposed within the high-speed clock source.

9. The clock control circuit of claim 2, wherein the high-speed clock source is structured so as to be able to select and output one high-speed clock from among a plurality of frequencies.

10. The clock control circuit of claim 4, further comprising a comparator which can be connected to an output side of the counter, and a register for setting a value corresponding to a stable time at a time of activation of the high-speed clock source in accordance with a control signal from the central processing unit,

wherein the register supplies an output signal to the comparator.

11. The clock control circuit of claim 5, wherein the flip-flop includes an input signal, a clock input, an asynchronous reset signal, and an output signal, and the low-through latch includes an input signal, a gate control signal, and a gate output, and when the reset input is a first signal, the gate output is reset in accordance with the first signal, and the gate output sets the input signal synchronously with a fall of the clock input.

12. The clock control circuit of claim 8, wherein the high-speed clock source can generate the high-speed clock, so as to select one frequency from among two or three or more frequencies.

13. The clock control circuit of claim 10, further comprising an OR gate which can be connected to an output side of the comparator, and a reset signal can be inputted to another input side of the OR gate, and an output side of the OR gate is connected to a set terminal of the flip-flop, and the selection signal can be outputted from the flip-flop.

14. A clock control method controlling a clock signal supplied to a central processing unit by a clock control circuit having a high-speed clock source whose oscillation operation is controlled by an operation control signal and which generates a

high-speed clock used in a usual operation mode, and a low-speed clock source always generating a low-speed clock whose frequency is lower than a frequency of the high-speed clock, the method comprising:

when a standby mode is designated by a mode signal, stopping the high-speed clock source, selecting the low-speed clock, and outputting the low-speed clock as the clock signal; and

when an interrupt signal is supplied, operating the high-speed clock source and starting counting of the low-speed clock, and when a count value reaches a set value, selecting the high-speed clock and outputting the high-speed clock as the clock signal.